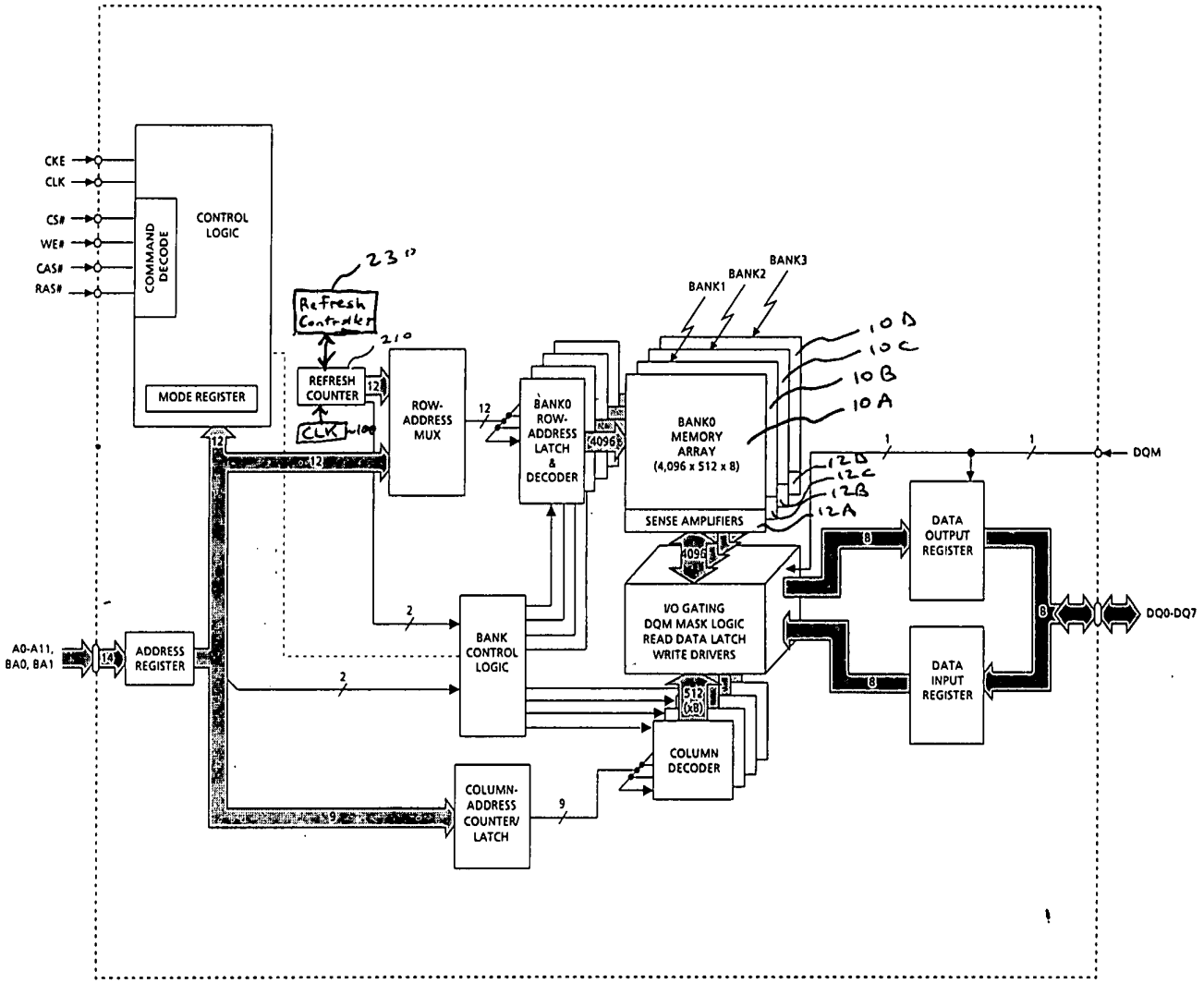

CKE
CLK
CS#
WE#
CAS#
RAS#
CONTROL LOGIC
COMMAND DECODE
MODE REGISTER
Refresh Controller
210
REFRESH COUNTER
CLK
ROW-ADDRESS MUX
BANK0 ROW-ADDRESS LATCH & DECODER
BANK0 MEMORY ARRAY (4,096 x 512 x 8)
BANK1
BANK2
BANK3
SENSE AMPLIFIERS
I/O GATING DQM MASK LOGIC READ DATA LATCH WRITE DRIVERS
DATA OUTPUT REGISTER
DATA INPUT REGISTER
DQM
DQ0-DQ7
A0-A11, BA0, BA1
ADDRESS REGISTER
BANK CONTROL LOGIC
COLUMN DECODER
COLUMN-ADDRESS COUNTER/ LATCH

Fig. 1

00T280"6TSTh960

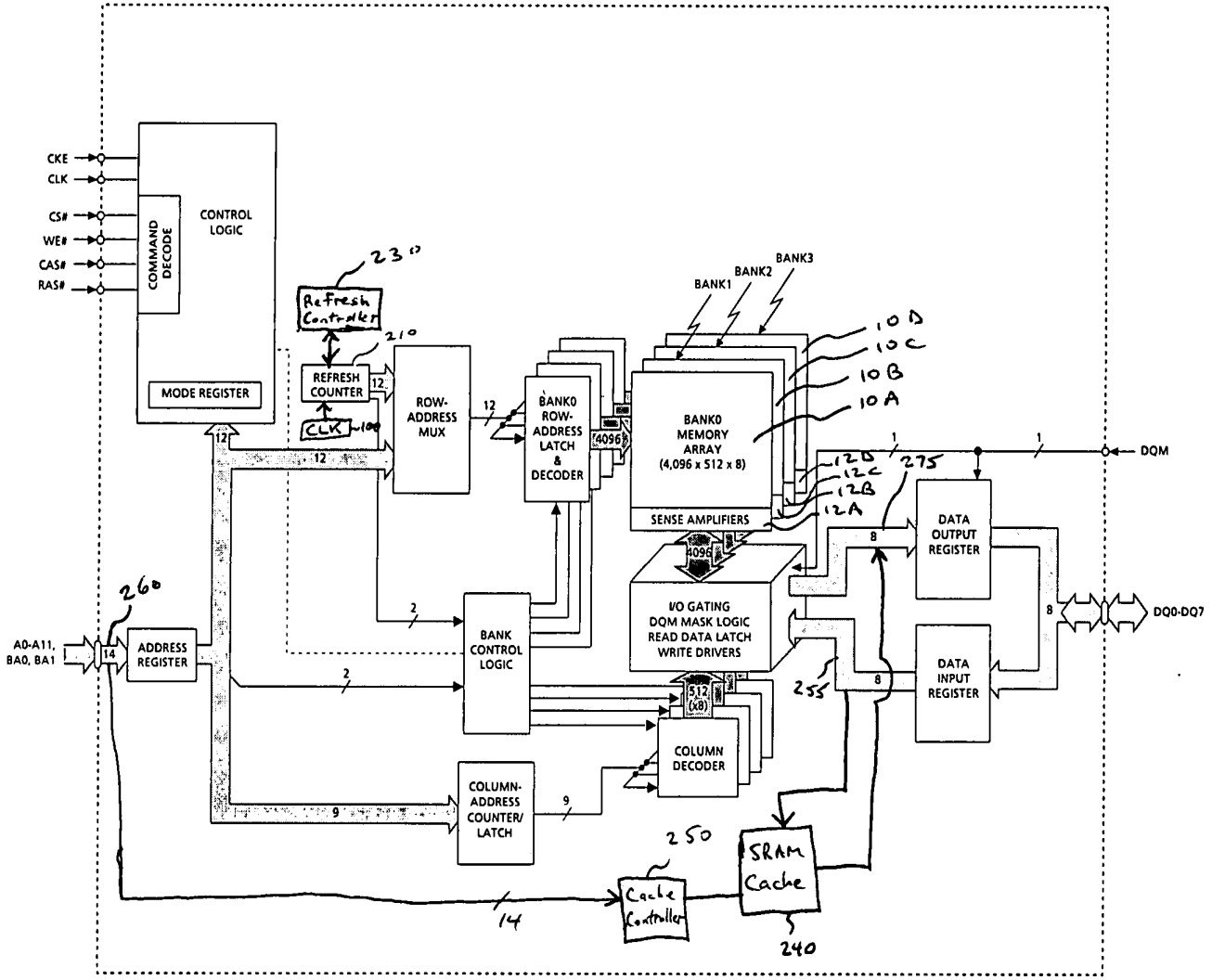
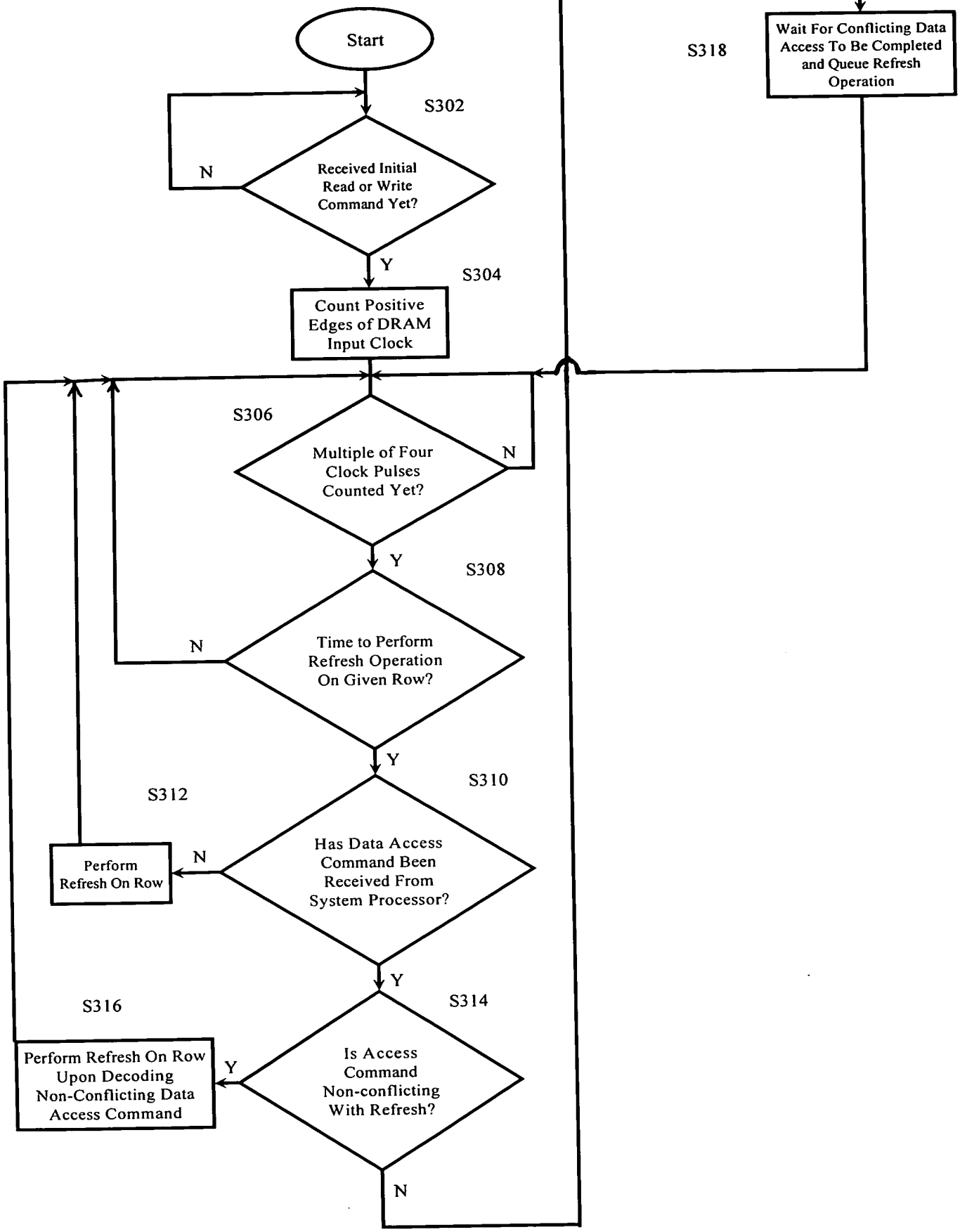



Fig. 2

Fig. 3


S300
Start
S302
Received Initial Read or Write Command Yet?
N
Y
S304
Count Positive Edges of DRAM Input Clock
S306
Multiple of Four Clock Pulses Counted Yet?
N
Y
S308
Time to Perform Refresh Operation On Given Row?
N
Y
S310
Has Data Access Command Been Received From System Processor?
N
S312
Perform Refresh On Row
Y
S314
Is Access Command Non-conflicting With Refresh?
Y
S316
Perform Refresh On Row Upon Decoding Non-Conflicting Data Access Command
N
S318
Wait For Conflicting Data Access To Be Completed and Queue Refresh Operation

READ - READ Timing Diagram

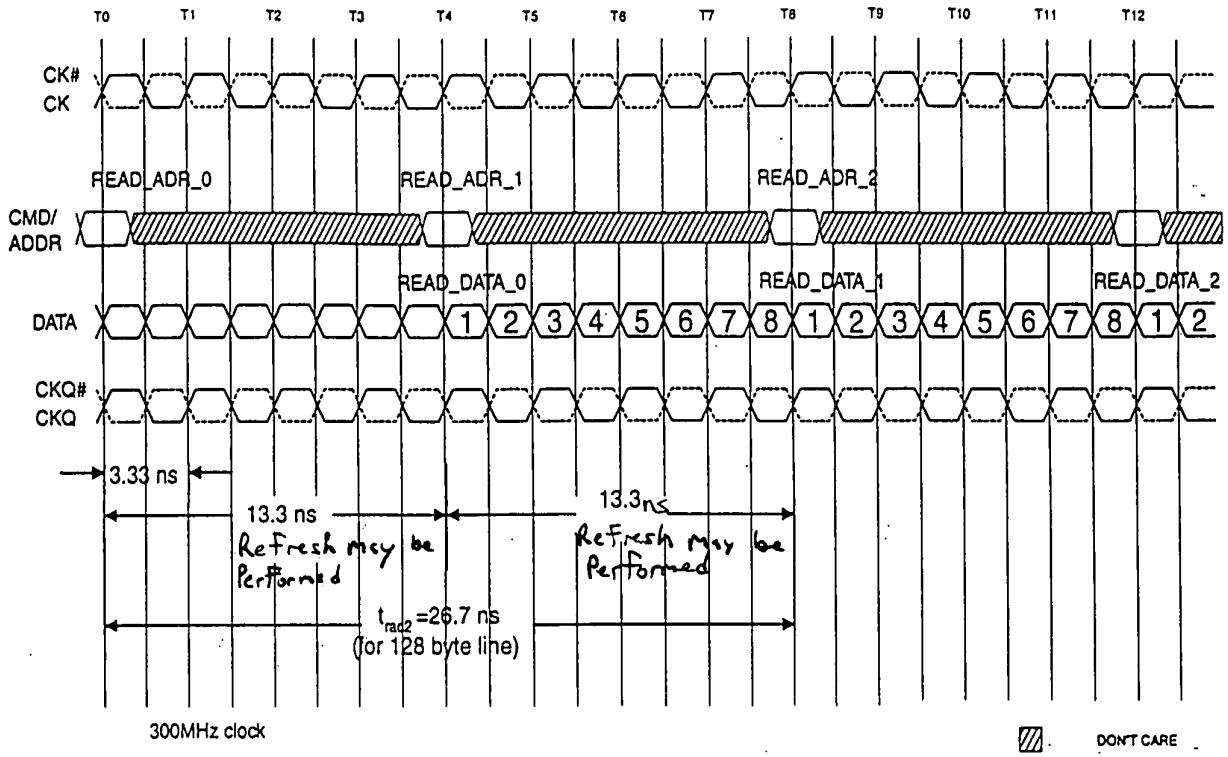



Fig. 4

0018280 "6T5Th960

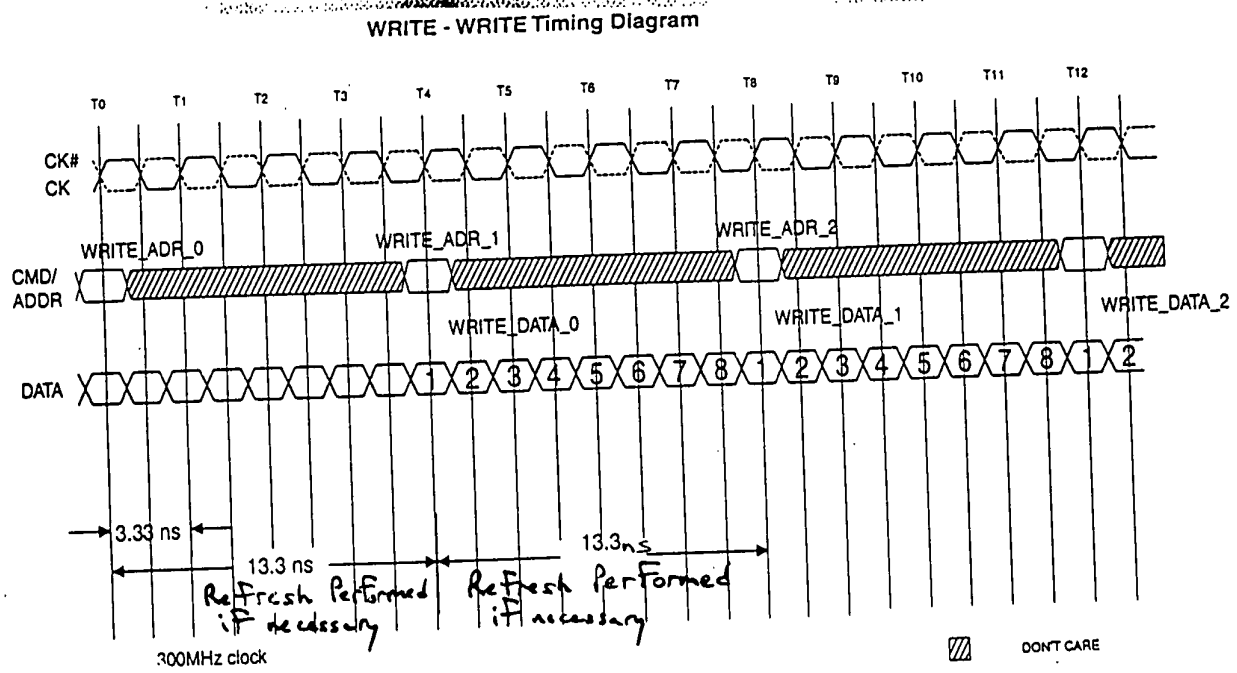



Fig. 5

**READ - WRITE - READ Timing Diagram**

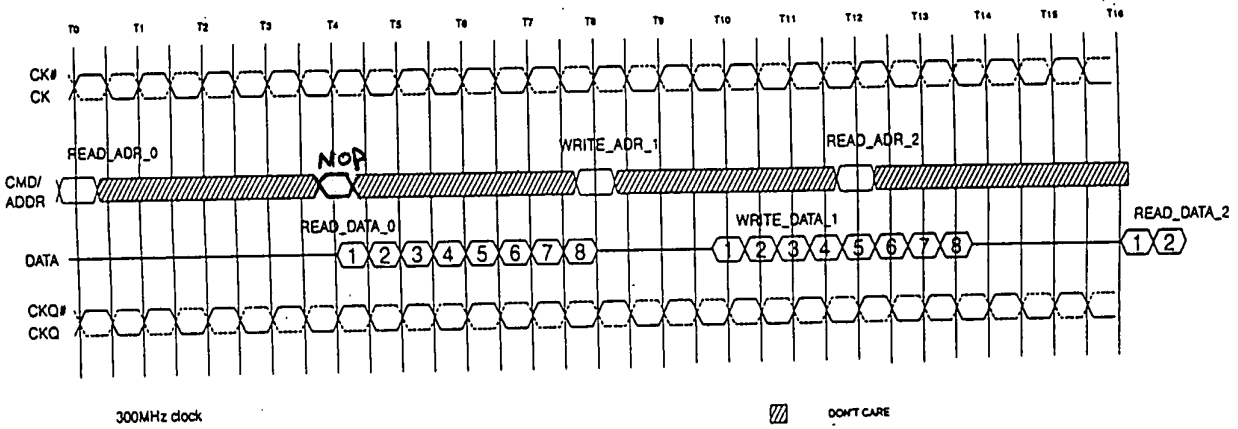



Fig. 6

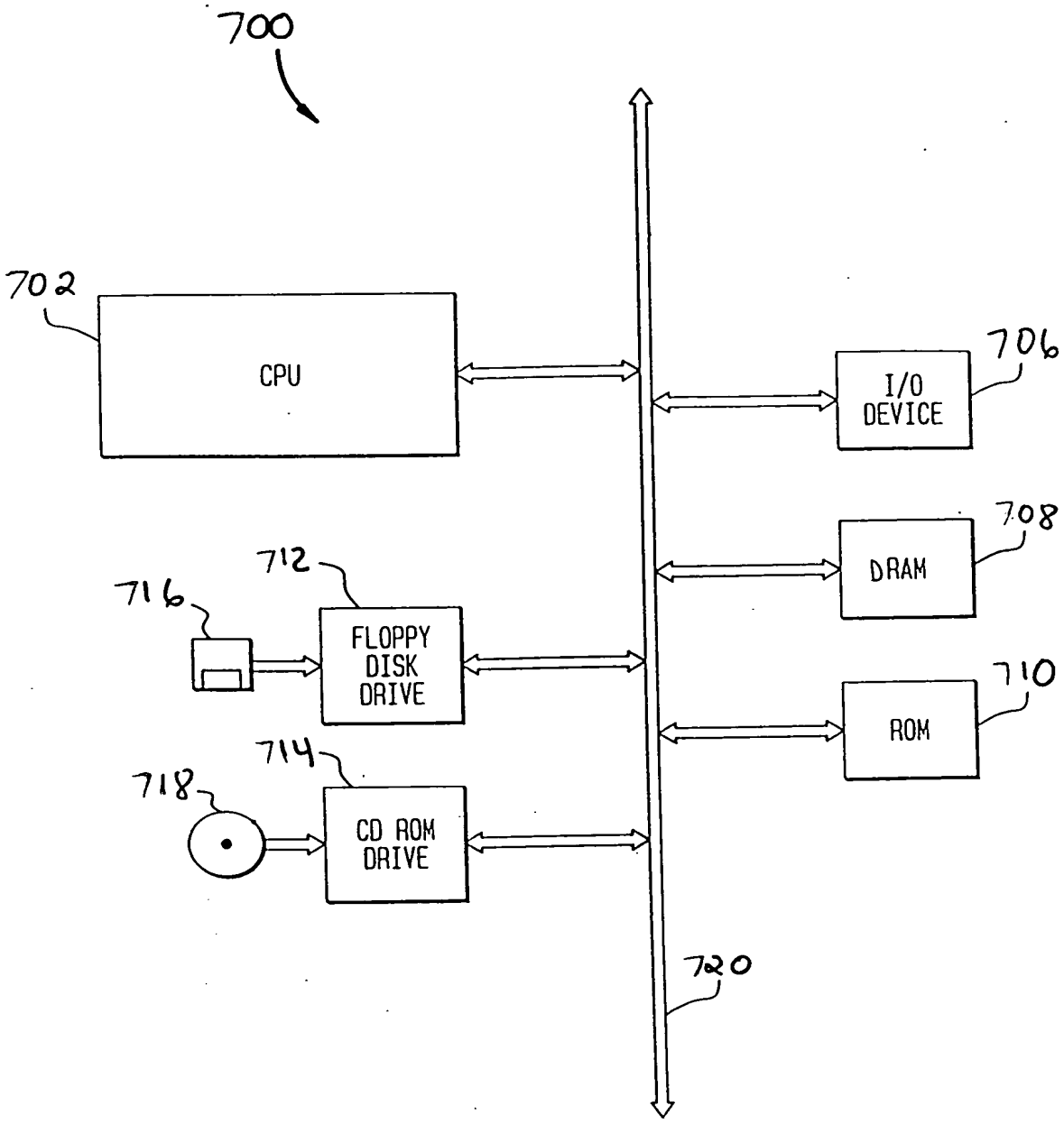

700
702
CPU
706
I/O DEVICE
708
DRAM
712
716
FLOPPY DISK DRIVE
710
ROM
714
718
CD ROM DRIVE
720

Fig. 7